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ACHIEVING AREA EFFICIENT PARALLEL FIR DIGITAL FILTER STRUCTURES FOR SYMMETRIC CONVOLUTIONS USING VLSI IMPLEMENTATION

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ABSTRACT

Based on fast finite impulse response(FIR) algorithms(FFAs) this paper proposes new parallel FIR filter structures, which are beneficial to symmetric coefficients in terms of the hardware cost, under the condition that the number of taps is a multiple of two or three and four. The main aim of this project is to achieve VLSI implementation using polyphase decomposition. The two, three and four tap parallel FIR filter is derived and then it can be represented as blocks. Exchanging multipliers with adders are advantageous because adders weigh less than multipliers in terms of silicon area. Hence we can reduce the hardware complexity. The proposed parallel FIR structures exploit the inherent nature of symmetric coefficients reducing half the number of multipliers in sub filter section at the expense of additional adders in preprocessing and post processing blocks. Hence 2, 3 and 4 parallel FIR filterimplementation is simulated through MATLAB (SIMULINK TOOL) AND XILINX (SYSTEM GENERATOR).

***IndexTerms*—**Digital Signal Processing (DSP),Fast Finite ImpulseResponse(FIR) Algorithm(FFAs), Matrix Laboratory (MATLAB), Polyphase Decomposition, Symmetric Convolutions, Subfilter, Symmetric Coefficients, Very Large Scale Integration(VLSI)

1. INTRODUCTION

Nowadays due to technological advancement, the demand for low-power and high-performance digital signal processing (DSP) is higher. A Finite Impulse response (FIR) filter is a filter whose response is of finite duration, because it settles to zero in finite time. Finite Impulse Response (FIR) digital filters are one of the most widely used basic devices in DSP systems for example video and image processing. Some applications need the FIR filter to operate at high frequencies such as video processing, whereas some other applications need high throughput with a low power circuit such as multiple-input multiple-output (MIMO) systems used in cellular telephony. When narrow transition- band characteristics are required, the much higher order in the FIR filter is unavoidable.On the other hand, parallel and pipelining are two techniques used in DSP applications which can be exploited to reduce the power consumption. Pipelining shortens the critical approach by interleaving pipelining latches along the data path, at the price of increasing the latches and system latency, whereas parallel processing increase the sampling rate by replicating hardware so that multiple inputs can be processed in parallel and multiple outputs are generated at the same time, at the expense of increasedarea. Both techniques reduce the power consumption by lowering the power supply, where the sampling speed does not increase. While the continuous trends in reducing chip area and integrate multi-chip solutions into a singlechipsolution, it is important to limit the silicon area required to implement parallel FIR digital filter in VLSI implementation.[ref 1997].In many design situations the hardware overhead incurred by parallel processing cannot be tolerated due to limitations in design area. Therefore, it is advantageous to realize parallel FIR filtering structures that consume less area than traditional parallel FIR filtering structures.[ref 1997].Due to its linear increase in the hardware implementation cost brought by the increase of the block size L, the parallel processing techniques loses its advantage in practical application. Therefore, our

goal is to take a comprehensive look at all of the aspects from filter design to implementation to produce low area parallel FIR filter structures. Polyphase decomposition is mainly manipulated, where the small-sized parallel FIR filter structures are derived first and then the larger block-sized ones can be constructed by cascading or iterating small sized parallel FIR filtering blocks.

2. FASR FIR ALGORITHM (FFA)

Consider an N-tap FIR filter which can be expressed in the general form as

$$y[n] = \sum_{I=0}^{N-1} h(i)\, x(n-i), \qquad n = 0,1,2 \ldots \infty \qquad (1)$$

Where {x(n)} is an infinite-length input sequence and {h(i)} are the length-N FIR filter coefficients. Then the traditional L-parallel FIR filter can be derived using polyphase decomposition as

$$\sum_{p=0}^{L-1} Y_p(Z)^L (Z)^{-p} = \sum_{q=0}^{L-1} X_q(Z)^L (Z)^{-q} + \sum_{r=0}^{L-1} H_r(Z)^L (Z)^{-r} \qquad (2)$$

Where $X_q = \sum_{K=0}^{\infty} z^{-K} x(LK+q)$, $H_r = \sum_{K=0}^{\left(\frac{N}{L}\right)-1} z^{-K} x\,(LK+r)$,

$Y_p = \sum_{K=0}^{\infty} z^{-K} x(LK+p)$, for p,q,r=0,1,2….L-1.From this FIR filtering equation, it shows that the traditional FIR filter will require L^2 − FIR subfilter blocks of length N/L for implementation.

EXISTING SYSTEM

A. 2×2 FFA (L=2)

According to (2),a two-parallel FIR filter can be expressed as

$$Y_0 + Z^{-1}Y_1 = (H_0 + Z^{-1}H_1)(X_0 + Z^{-1}X_1) = H_0X_0 + Z^{-1}(H_0X_1 + H_1X_0) + Z^{-2}H_1X_1 \qquad (3)$$

Implying that

$$Y_0 = H_0X_0 + Z^{-2}H_1X_1, \quad Y_1 = H_0X_1 + H_1X_0. \qquad (4)$$

Equation (4)

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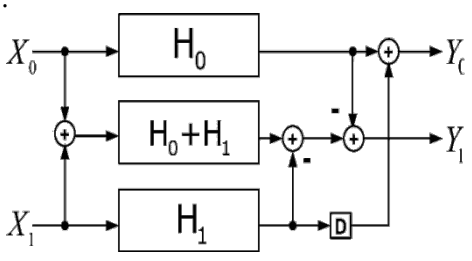


Fig.1. Two-parallel FIR filter implementation using FFA.

Equation(4)shows the traditional two-parallel filter structure, which will require four length-N/2 subfilter blocks, two postprocessing adders, and totally 2N multipliers and 2N-2 adders. However (4) can be written as

$$Y_0 = H_0X_0 + Z^{-2}H_1X_1,$$
$$Y_1 = (H_0 + H_1)(X_0 + X_1) - H_0X_0 - H_1X_1 \qquad (5)$$

The implementation of(5) will require three FIR subfilter blocks of length N/2, one preprocessing and three postprocessing adders, and3N/2 multipliers and 3(N/2-1)+4 adders,which reduces approximately one fourth over the traditional two-parallel filter hardware cost from(4).The twoparallel (L=2) FIR filterimplementation using FFA obtained from (5) is shown in Fig.1.

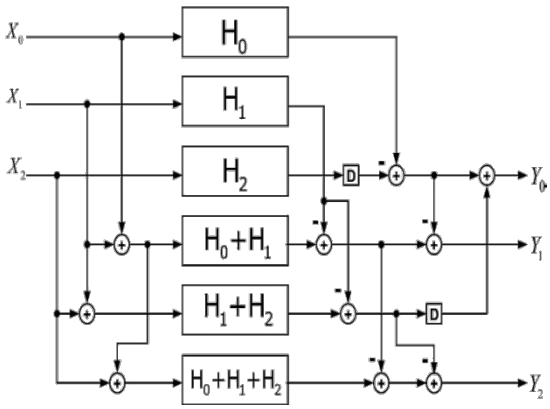


Fig.2.Three-parallel FIR filter implementation.

B. 3×3 FFA (L=3)

By the similar approach, a three-parallel FIR filter using FFA can be expressed as

$$Y_0 = H_0X_0 - Z^{-3}H_2X_2 - Z^{-3}[(H_1 + H_2)(X_1 + X_2) - H_1X_1]$$

$$Y_1 = [(H_0 + H_1)(X_0 + X_1) - H_1X_1] - (H_0X_0 - Z^{-3}H_2X_2)$$

$$Y_2 = [(H_0 + H_1 + H_2)(X_0 + X_1 + X_2)] - [H0+H1)(X0+X1-H1X1-[(H1+H2)(X1+X2)-H_1X_1] \qquad (6)$$

The hardware implementation of (6) requires six length-N/3 FIRsubfilter blocks,three preprocessing and seven postprocessing adders, and three N multipliers and 2N+4 adders, which has reduced approximately one third over the traditional three-parallel filter hardware cost. The implementation obtained from (6) is shown in Fig.2.

C. 4×4 FFA (L=4)

By the similar approach, a four parallel FIR filter using FFA can be expressed as

$$Y_0 + Y_1Z^{-1} + Y_2Z^{-2} + Y_3Z^{-3} = H_0X_0 + Z^{-1}(H_0X_1 + H_1X_0) + Z^{-2}(H_0X_2 + H_1X_1 + H_2X_0) + Z^{-3}(H_1X_2 + H_0X_3 + H_3X_0 + H_2X_1) + Z^{-4}(H_1X_3 + H_2X_2 + H_3X_1) + Z^{-5}(H_2X_3 + H_3X_2) + Z^{-6}(H_3X_3) \quad (7)$$

3.PROPOSED FFA STRUCTURES FOR SYMMETRIC CONVOLUTIONS.

By utilizing the symmetry of coefficients properly, the main idea behind the proposed structures is intuitive, to manipulate the polyphase decomposition to earn as many subfilter blocks as possible which contain symmetric coefficients so that half the number of multiplications in the single subfilter block can be reused for the multiplications of whole taps.

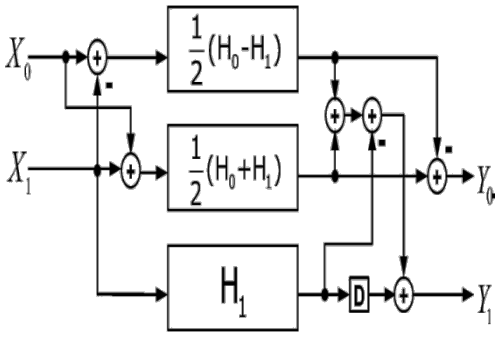


Fig.3. Proposed two-parallel FIR filter implementation.

Therefore, for an N-tap L-parallel FIR filter the total amount of saved multipliers would be the number of subfilter blocks that contain symmetric coefficients times half the number of multiplications in a single subfilter block(N/2L).

A. 2×2 Proposed FFA (L=2)

From (4), a two-parallel FIR filter can also be written as

$$Y_0 = \{1/2[(H_0 + H_1)(X_0 + X_1) + (H_0 - H_1)(X_0 - X_1)] - H_1X_1\} + Z^{-2}H_1X_1$$

$$Y_1 = \{1/2[(H_0 + H_1)(X_0 + X_1) - (H_0 - H_1)(X_0 - X1(8)$$

When it comes to a set of even symmetric coefficients, (7) can earn one more subfilter block containing symmetric coefficients than (5), the existing FFA parallel FIR filter.Fig.3 shows implementation of the proposed two-parallel FIR filter based on (8).The clear perspective of subfilter blocks are analysed using below equation as

$$h[n] = h[M - 1 - n,\ n = 0,1,2, \dots \dots N - 1 \quad (9)$$

B. 3×3 Proposed FFA (L=3)

Using similar approach (6), a three parallel FIR filter can also be written as (10).Fig. 4 shows implementation of the proposed three-parallel FIR filter. When the number of symmetric coefficients N is multiple of 3, the proposed three-parallel FIR filter structure presented in (9) enables four subfilter blocks with symmetric coefficients in total,whereas the existing FFA parallel fir filter structure has only two ones out of six subfilter blocks. The three parallel FIR filter can also be written as

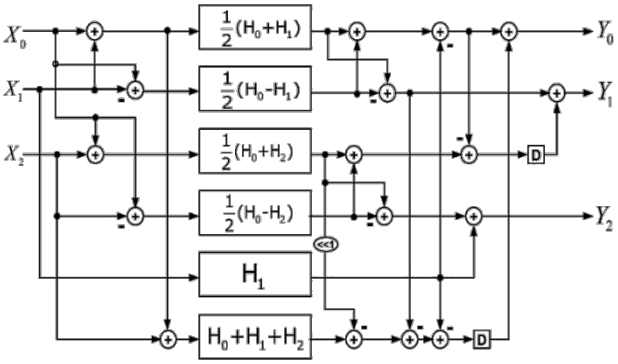
$$Y_0 = 1/2[(H_0 + H_1)(X_0 + X_1) + (H_0 - H1)(X0-X1-H1X1+Z-3\{(H0+H1+H2)(X0+X1+X2)\text{-}H0+H2)(X0+X2)-1/2[(H_0 + H_1)(X_0 + X_1) - (H_0 - H_1)(X_0 - X_1)]-H_1X_1\}$$

$$Y_1 = 1/2[(H_0 + H_1)(X_0 + X_1) - (H_0 - H1)(X0-X1+Z-3\{½H0+H2(X0+X2+H0-H2(X0-X2]]-1/2[H0+H1)(X0+X1+H0-H1)(X0-X1+H1X1$$

$$Y_2 = \{1/2[(H_0 + H_2)(X_0 + X_2) - (H_0 - H_2)(X_0 - X2+H1X1$$

(10)

Therefore,for an N-tap three parallel FIR filter, the proposed structure can save N/3 multipliers from the existing FFA structure.However, again, the proposed three-parallel FIR structure also brings an overhead of seven additional adders in preprocessing and postprocessing blocks.



4. SIMULINK AND SYSTEM GENERATOR DETAILS

The simpleimplementation of two parallel FIR filter structures are given below as example as

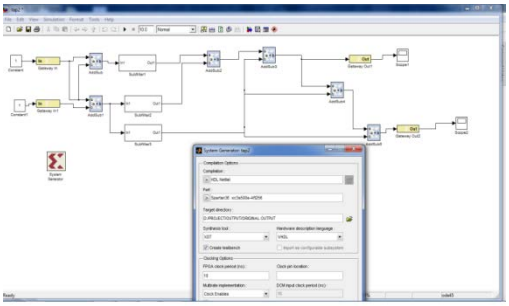


Fig.4.Two parallel FIR filter implementation in SIMUINK

The device utilization of two parallel digital FIR filter is given below as

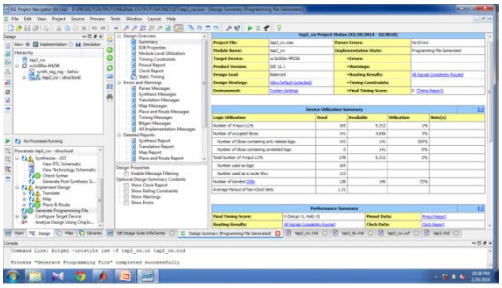


Fig.5.Device utilization of two parallel digital FIR filter.

After efficient derivation from equation (10), the SIMULINK block diagram is implemented. The SIMULINK representation of four parallel FIR filter structure is given below as

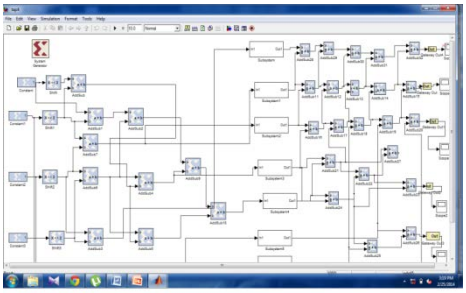


Fig.6. SIMULINK representation of four parallel FIR filter.

After implemented in SIMULINK, we will get the required the language(VHDL,VERILOG) netlist files from SYSTEM GENERATOR tool in XILINX.

When an L-parallel FIR filter comes with a set of symmetric coefficients of length N, the number of required multipliers for the proposed parallel FIR filter structures are provided by (11) and (12).

Case I:

When $N/\prod_{i=1}^{r} Li$ is even,

$$M = N/\prod_{i=1}^{r} Li \left(\prod_{i=1}^{r} Mi - S/2\right) \quad (11)$$

Case II:

When $N/\prod_{i=1}^{r} Li$ is odd,

$$M = N/\prod_{i=1}^{r} Li \left(\prod_{i=1}^{r} Mi - S/2\right)\left(\frac{N}{\prod_{i=1}^{r} Li} - 1\right) \quad (12)$$

The number of the required adders in subfilter section can be given by

$$Asub = \prod_{i=1}^{r} Mi\left(\frac{N}{\prod_{i=1}^{r} Li} - 1\right) \quad (13)$$

5. FUTURE WORK AND CONCLUSION

In this paper we have presented new paralle FIR filter structures, which are beneficial to symmetric convolutions when the number of taps is the multiple of 2,3 and 4 using SIMULINK and SYSTEM GENERATOR tool. For future work, by using efficient derivation for 5 and 6 tap parallel FIR filter structures .Overall, in this paper, we have provided new simulated structure for multiple tap of parallel FIR filter structures consisting of advantageous polyphase decompositions dealing with symmetric convolutions.

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